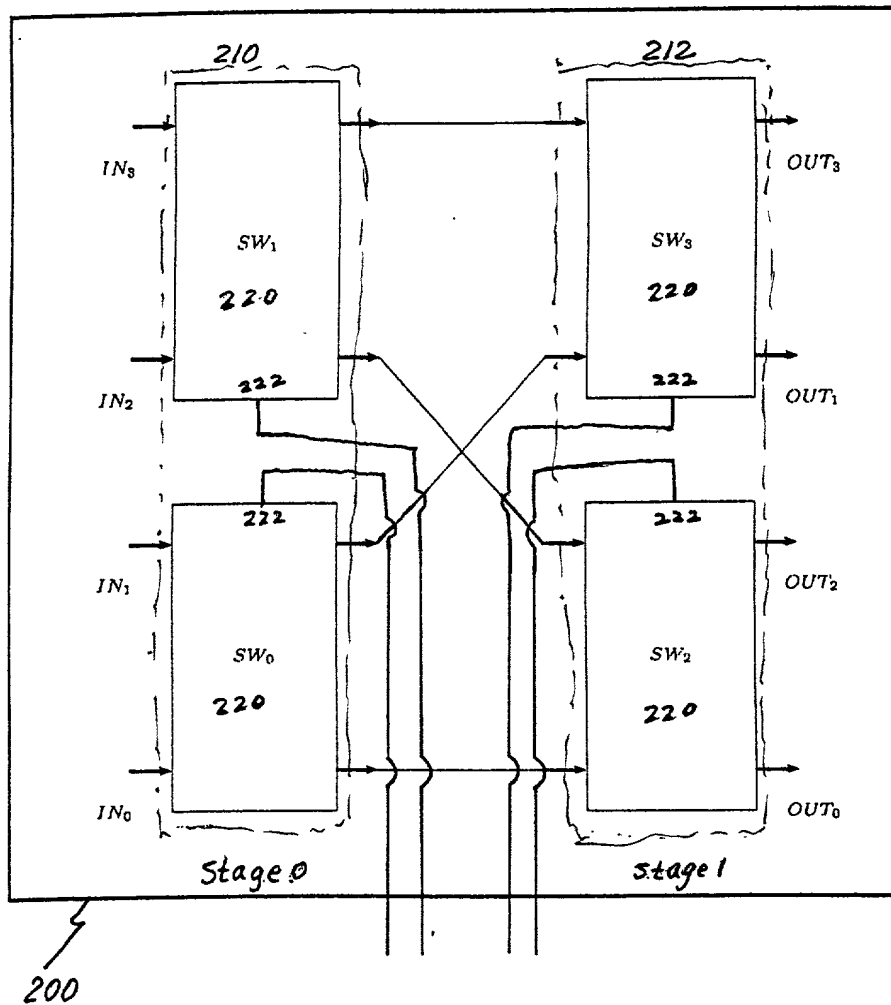


Fig. 1. (Prior Art)



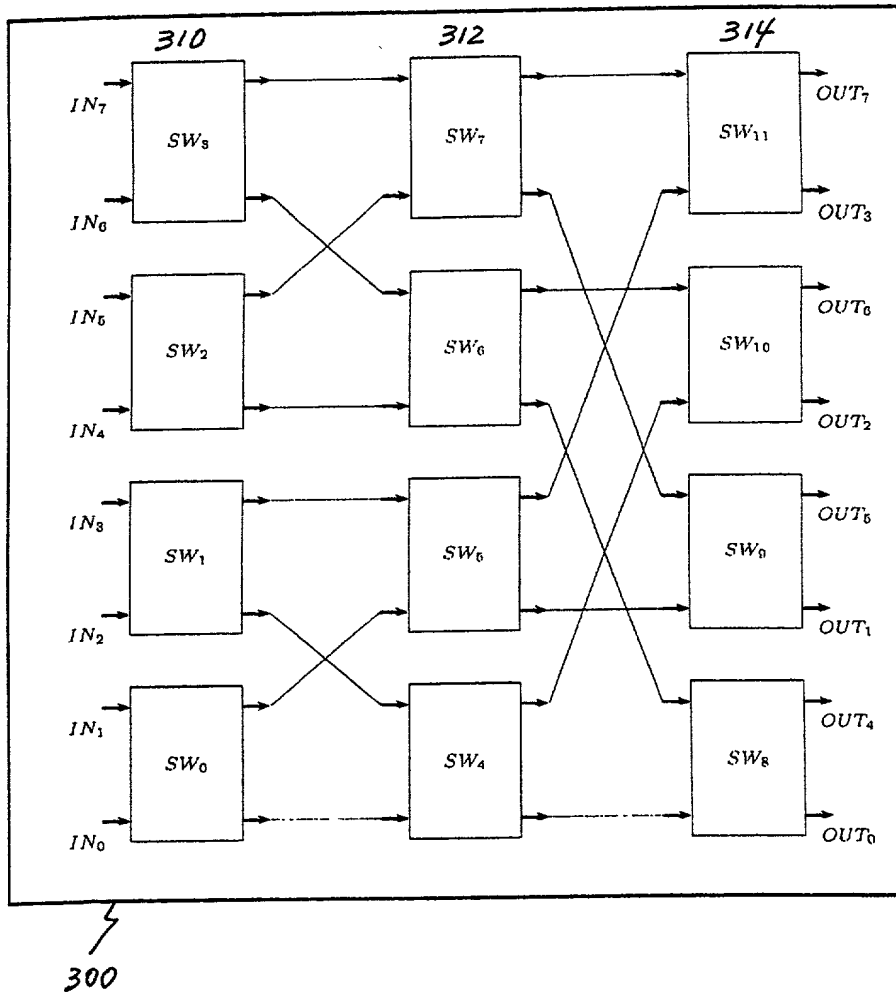


Fig 3

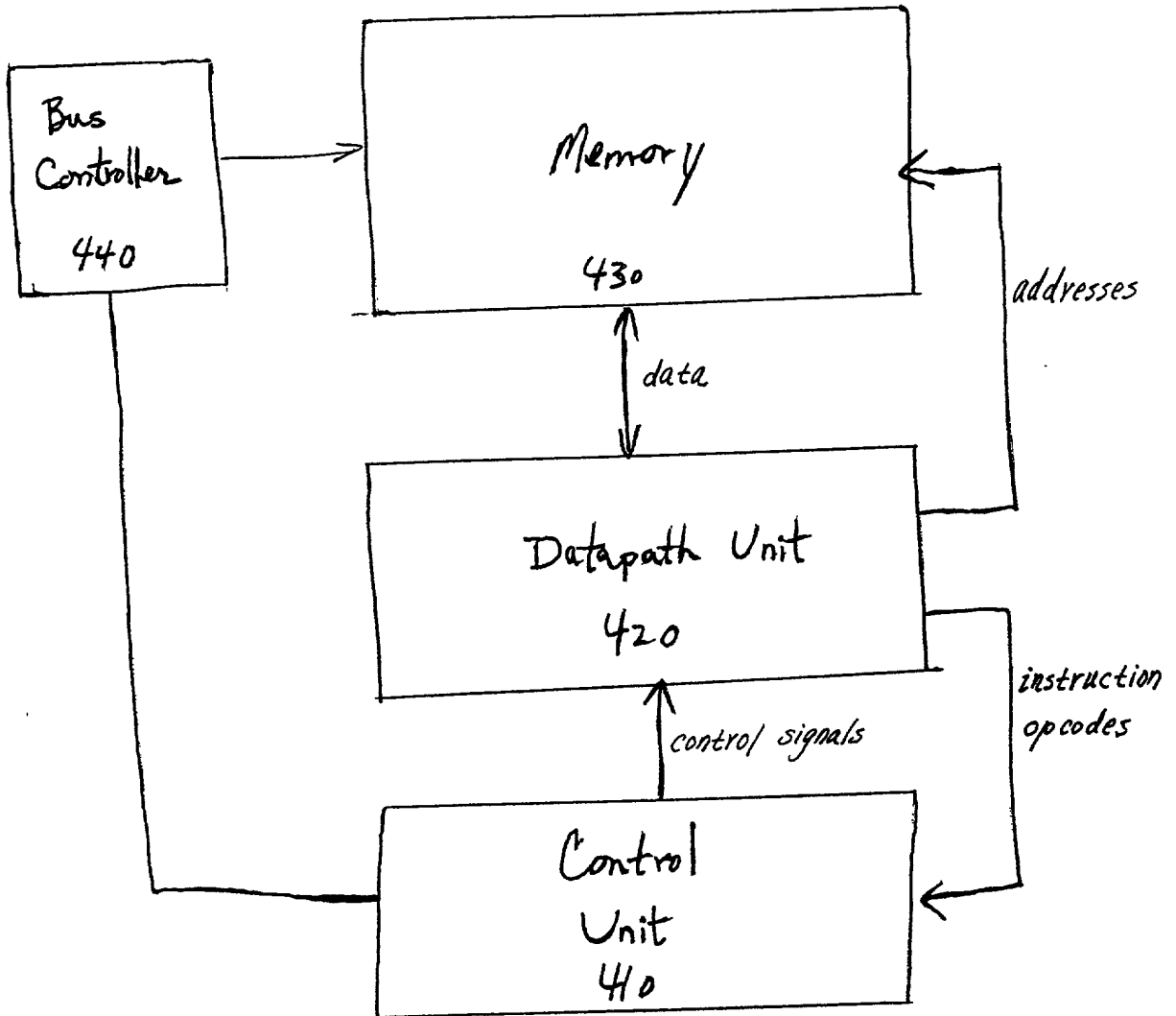


Figure 4

400 ↗

FIG. 5 is a block diagram of a Banyan Switched Processor Datapath, showing the internal components and their interconnections. The diagram is enclosed in a dashed box 420.

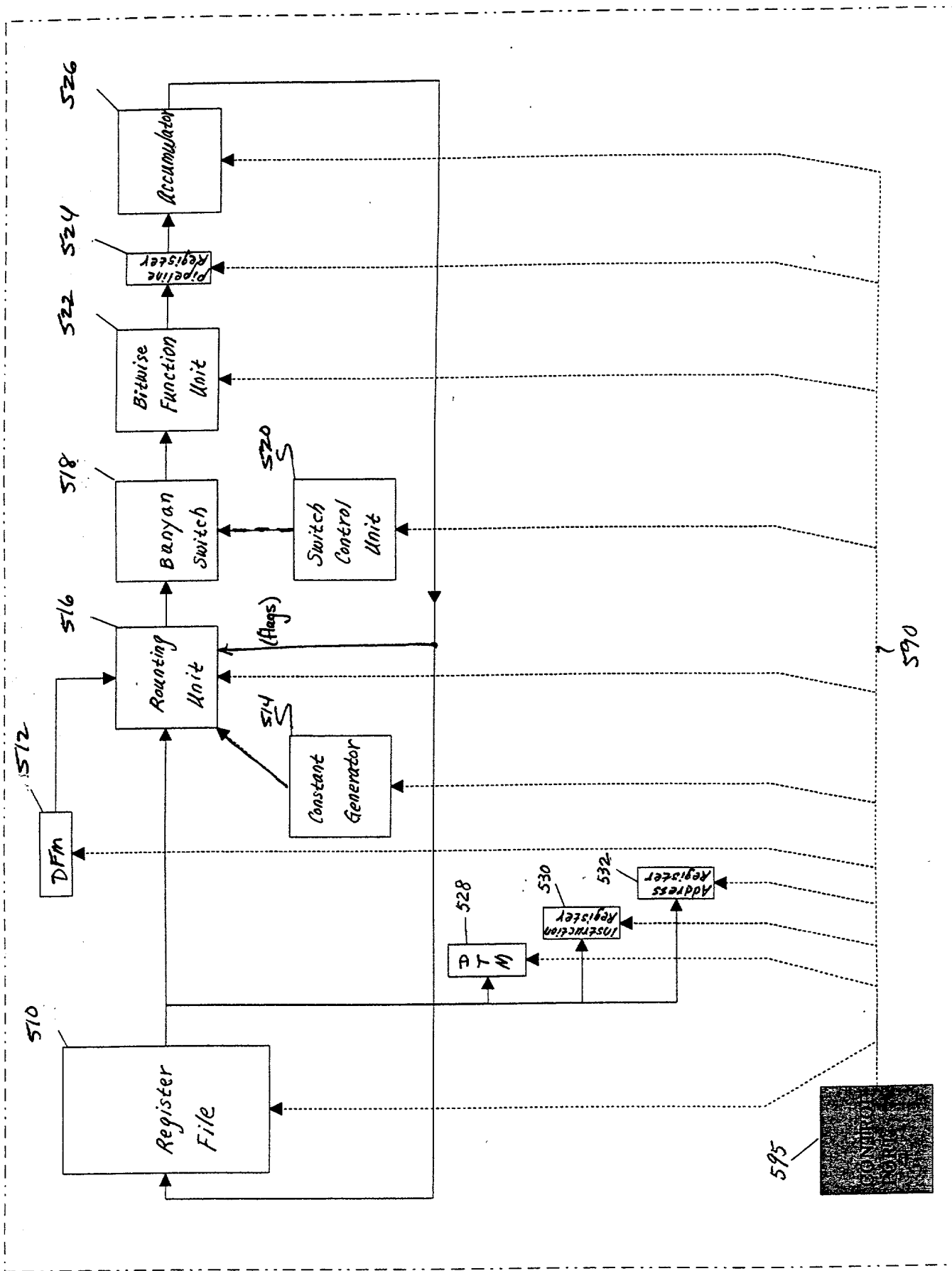


Fig. 5

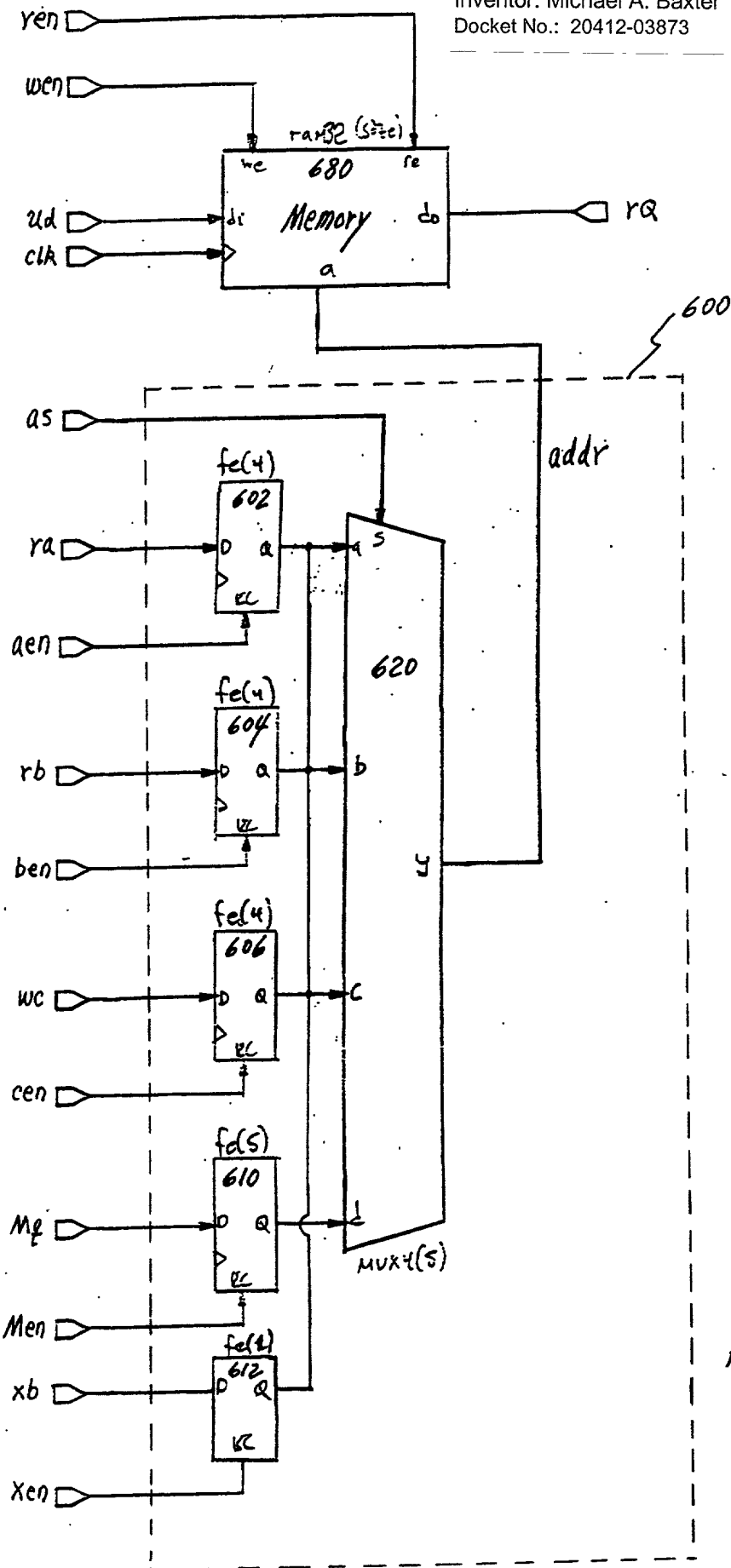


Figure 6A

[illegible]

## Function 0

Data from memory, to be passed through switch without rotation.

## Function 1

$V_k$  literal for AK instruction, to be passed through switch, without rotation, pre-aligned left of  $2^5$ .

$V_k$  literal for SK instruction, to be passed through switch, without rotation, pre-aligned left of  $Z$ .

Insert PCW Flag

SK<sub>16</sub> sign-extended, to be rotated RLC(4), with zero-fill pre-appended.

64-bit constants bus.

64-bit register file read bus.

Force KISA-2 out.

### Figure 6B

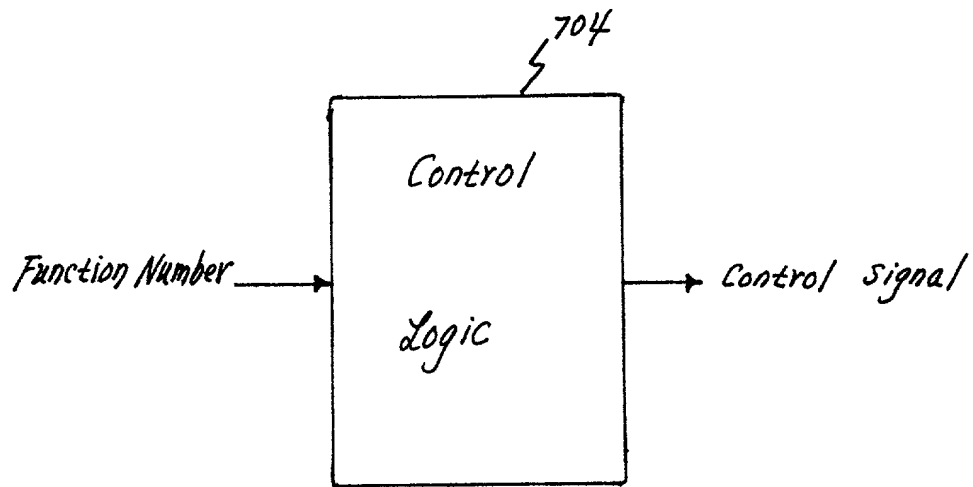
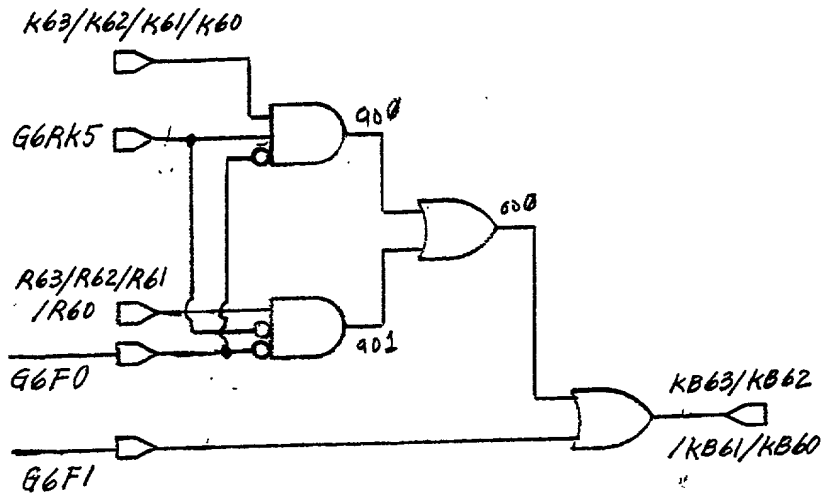


Figure 7A





710

Figure 7B

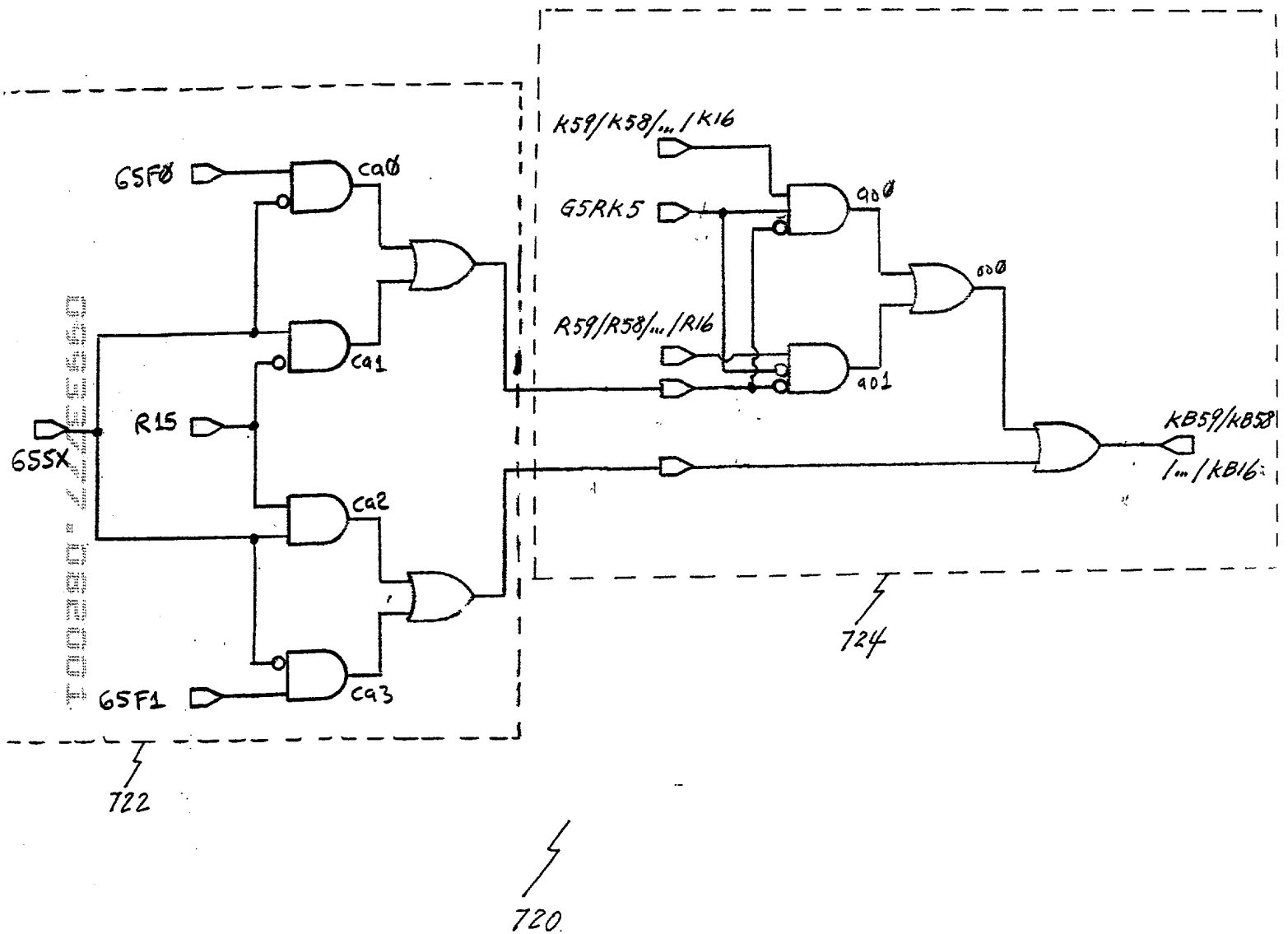
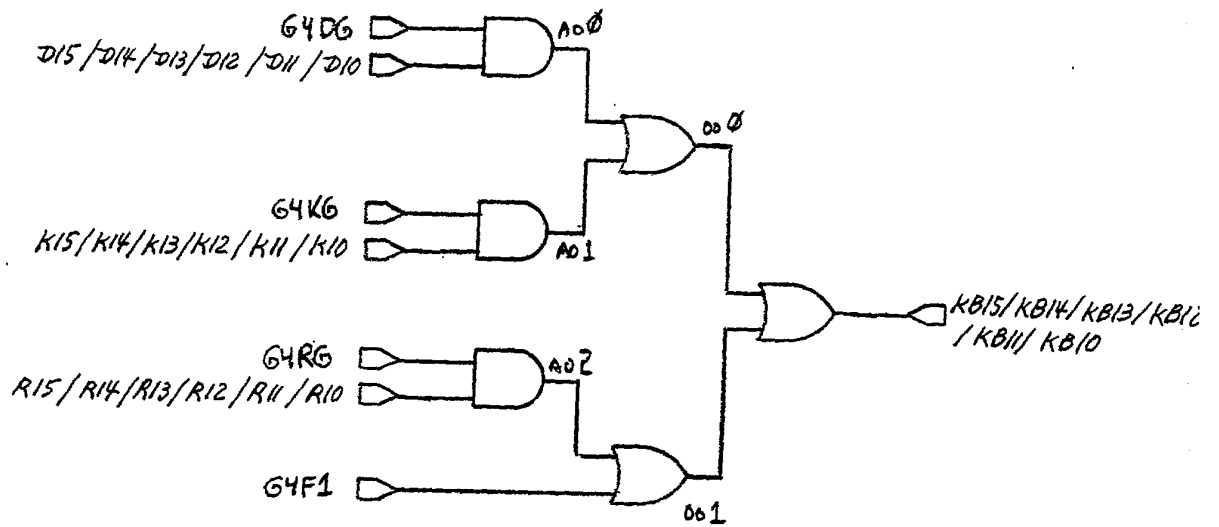


Figure TC



730

Figure 7D

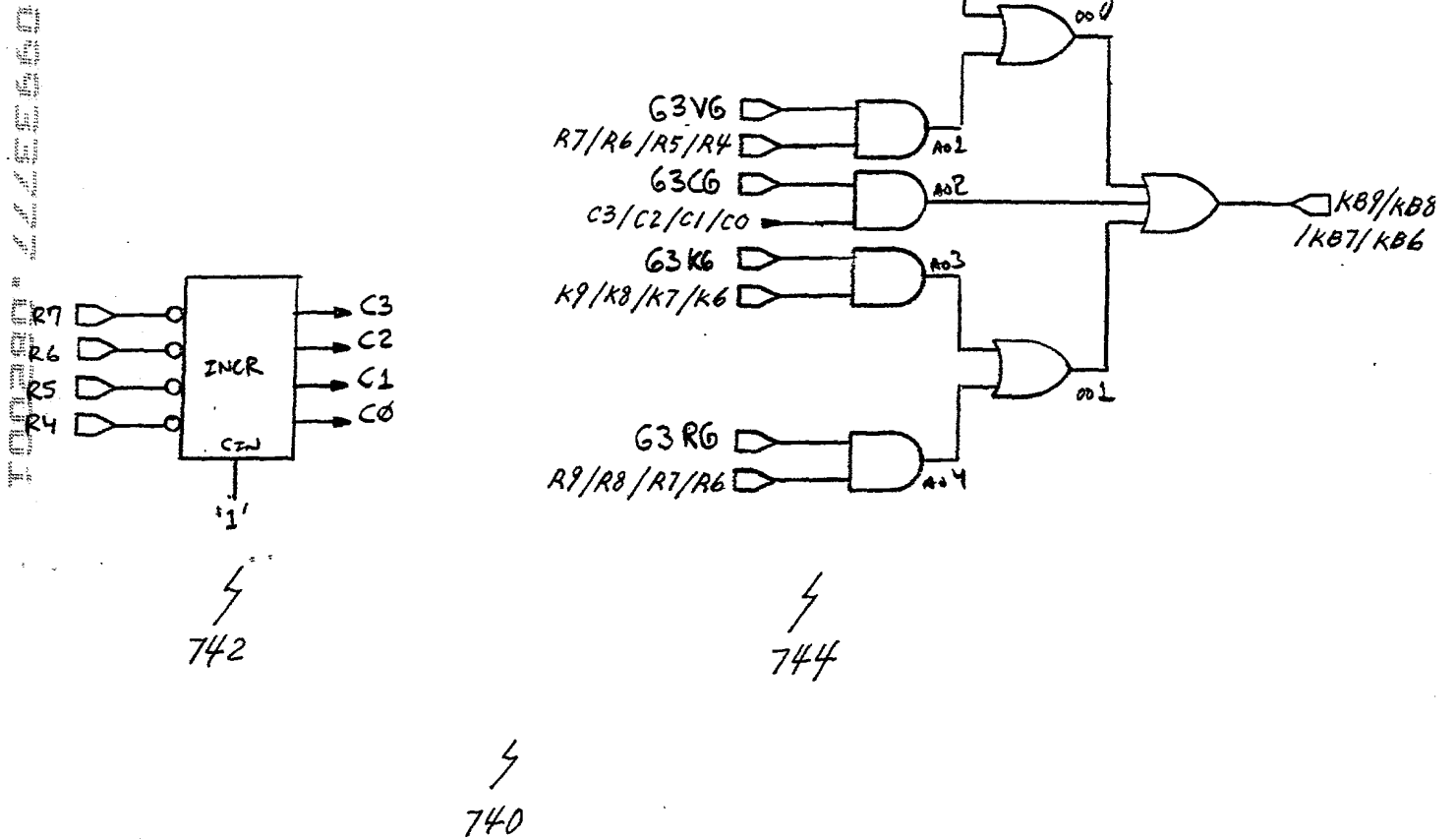
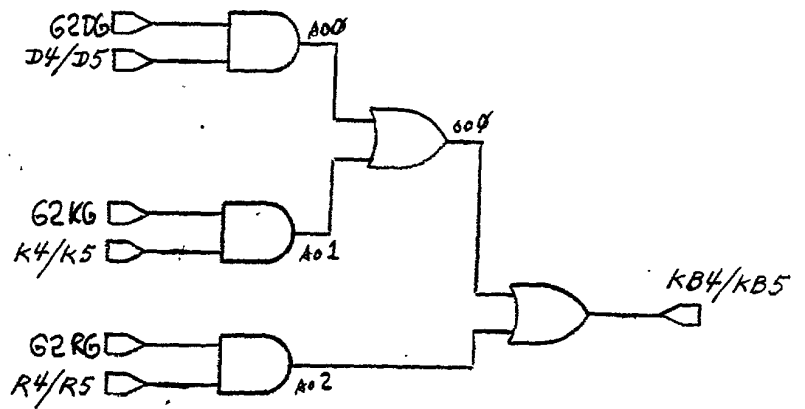
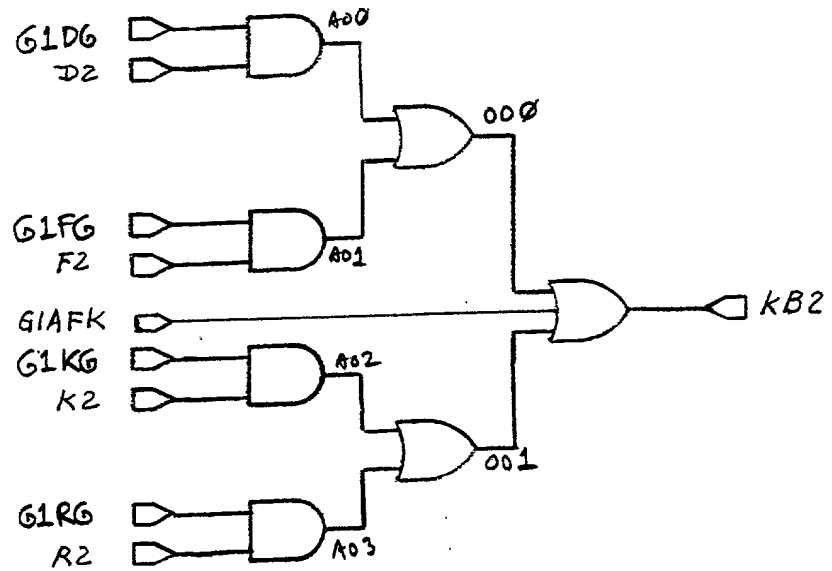


Figure 7E



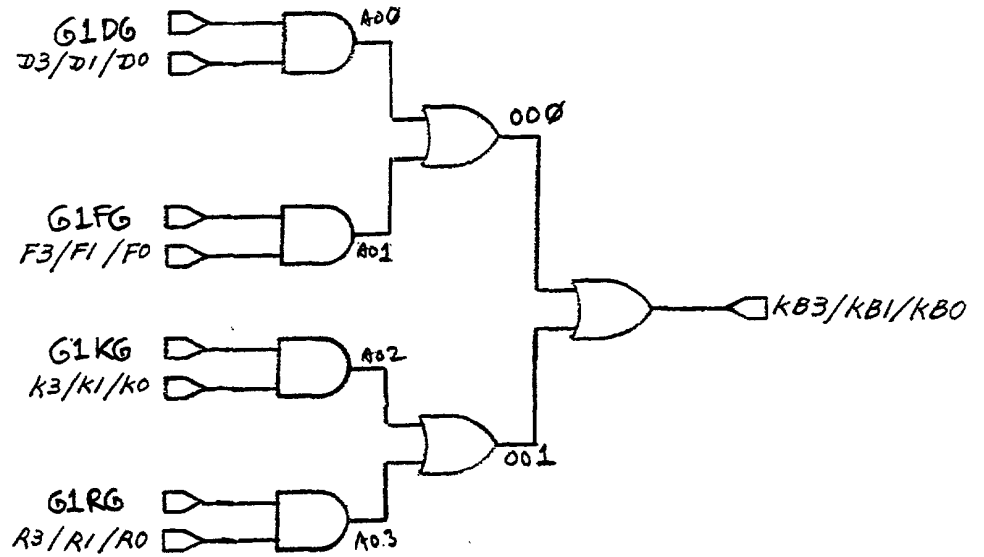
750

Figure 7F



760

Figure 7G



770

Figure 7H

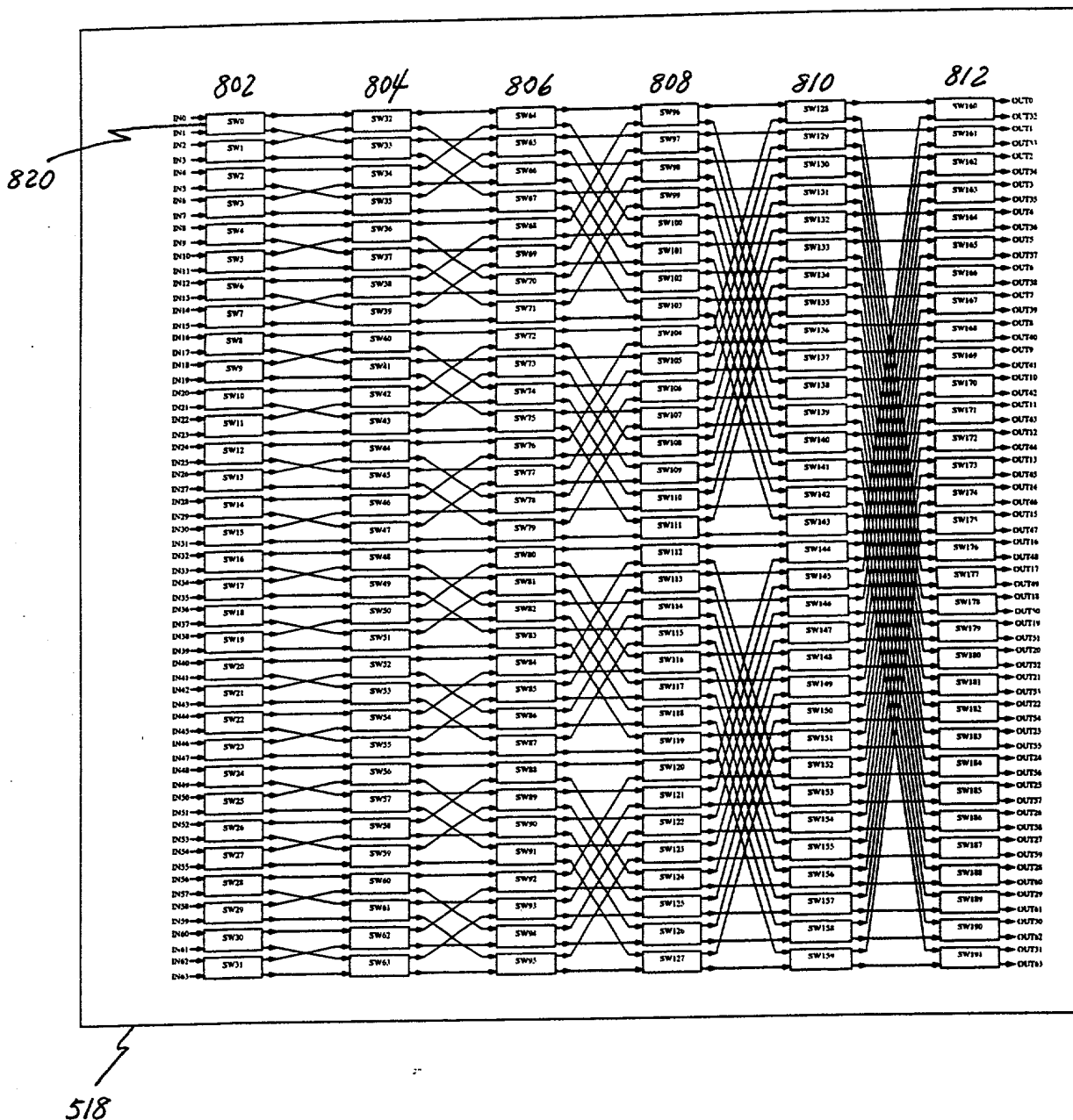


Fig. 8



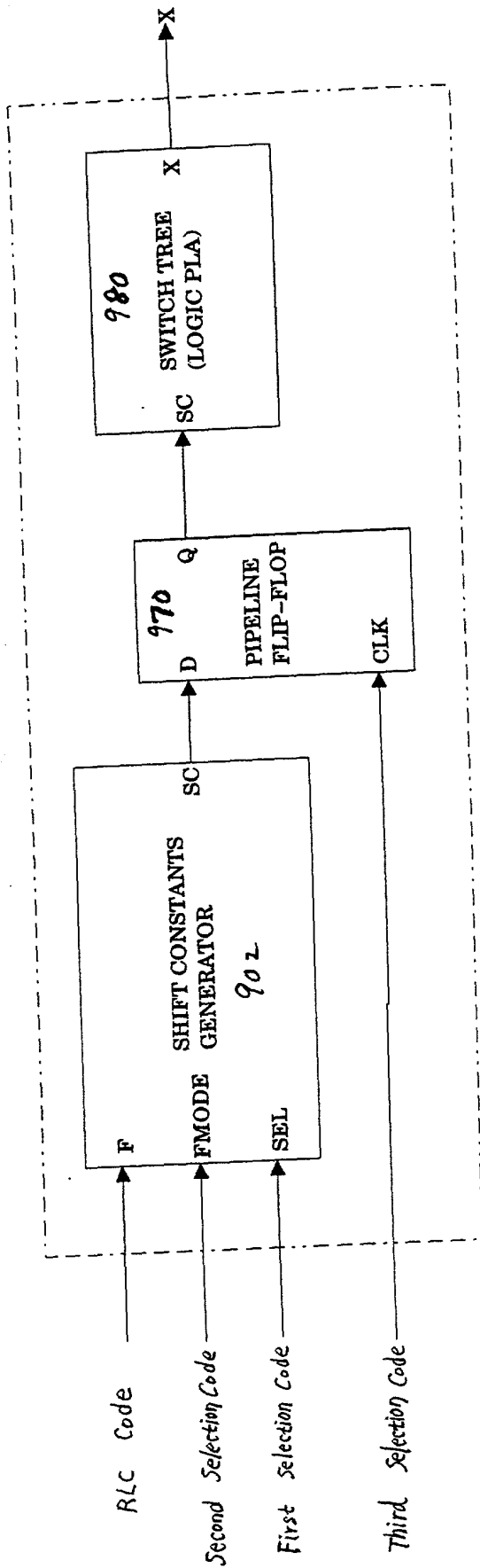


Fig. 9A

7  
520

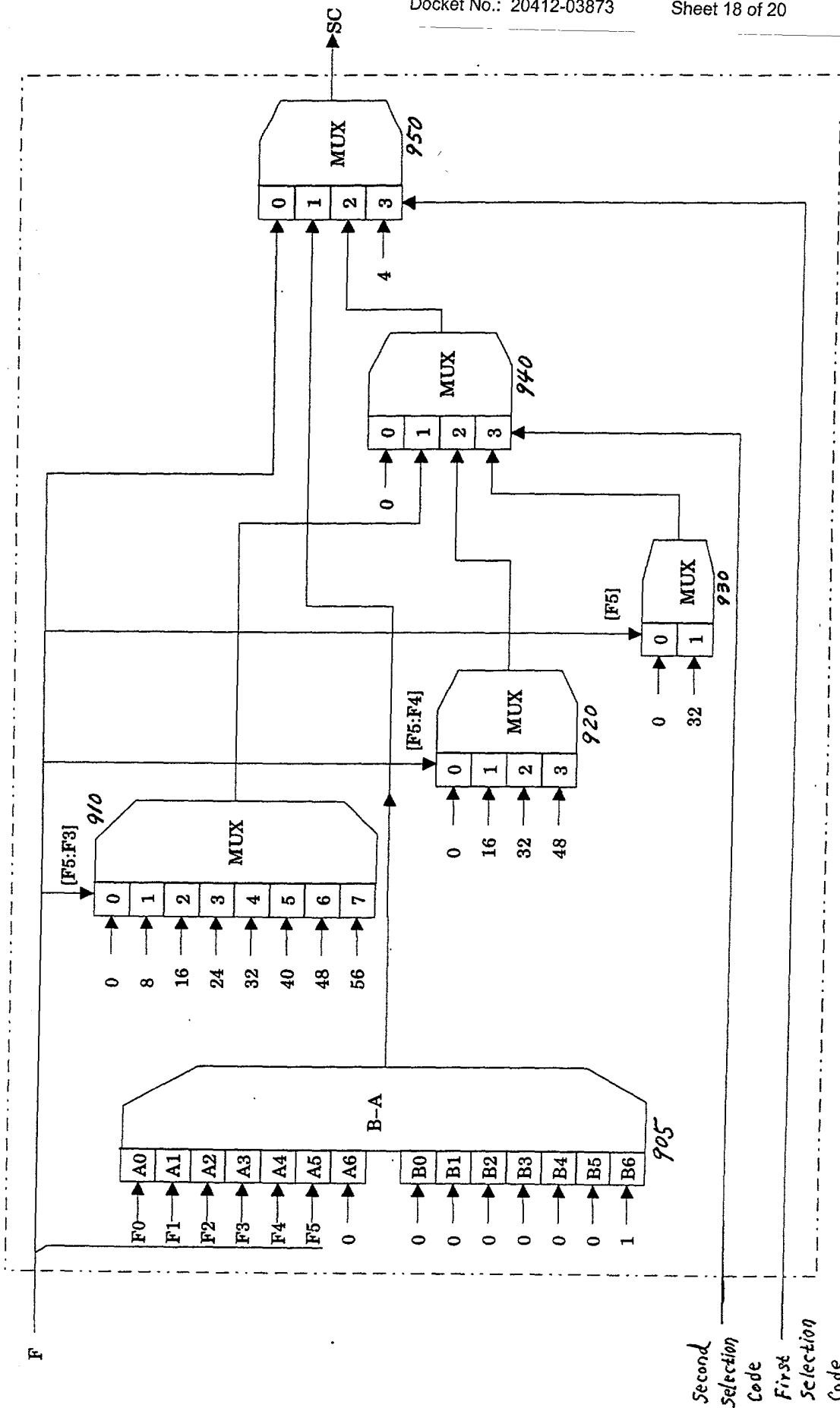


Fig. 9B

902

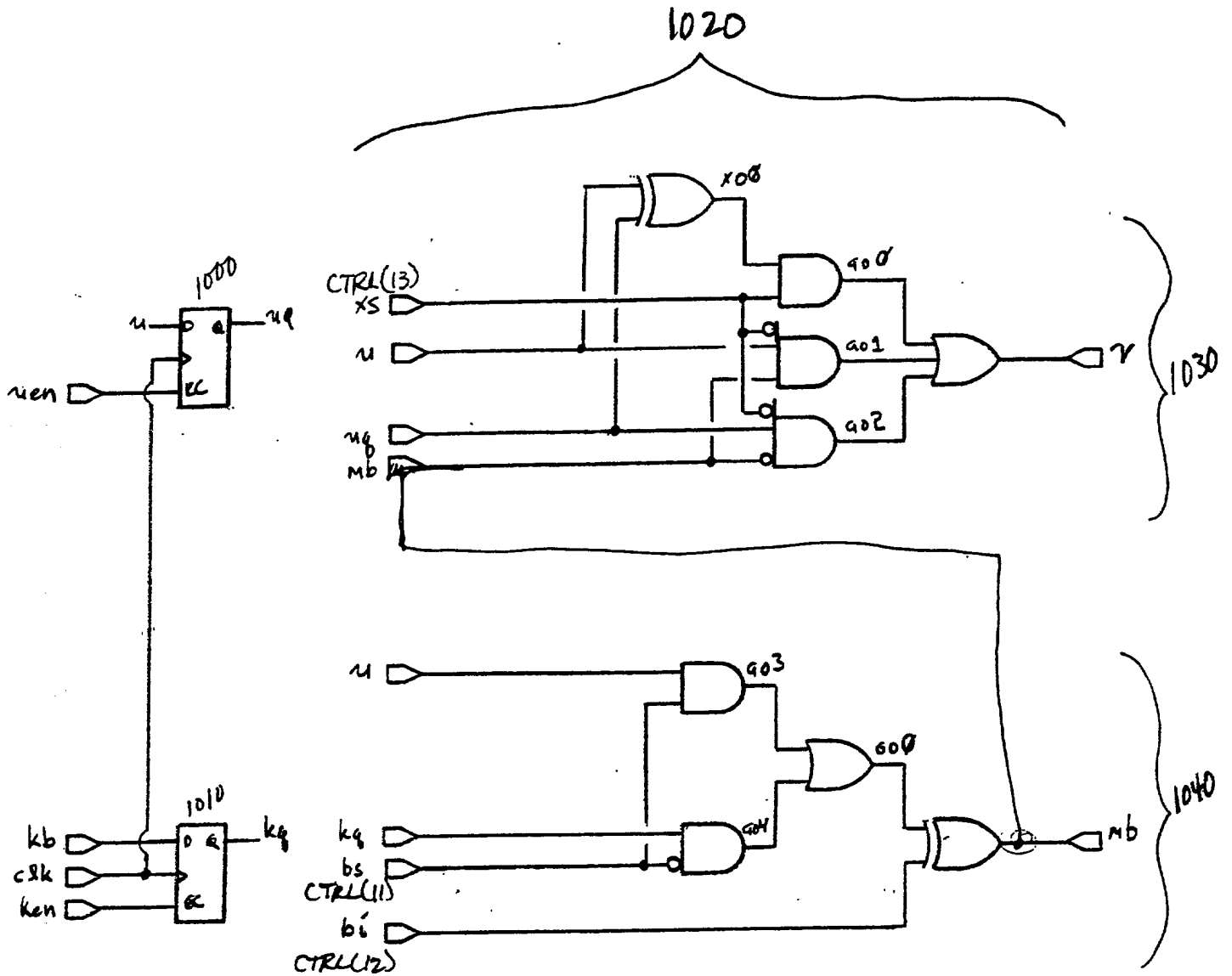
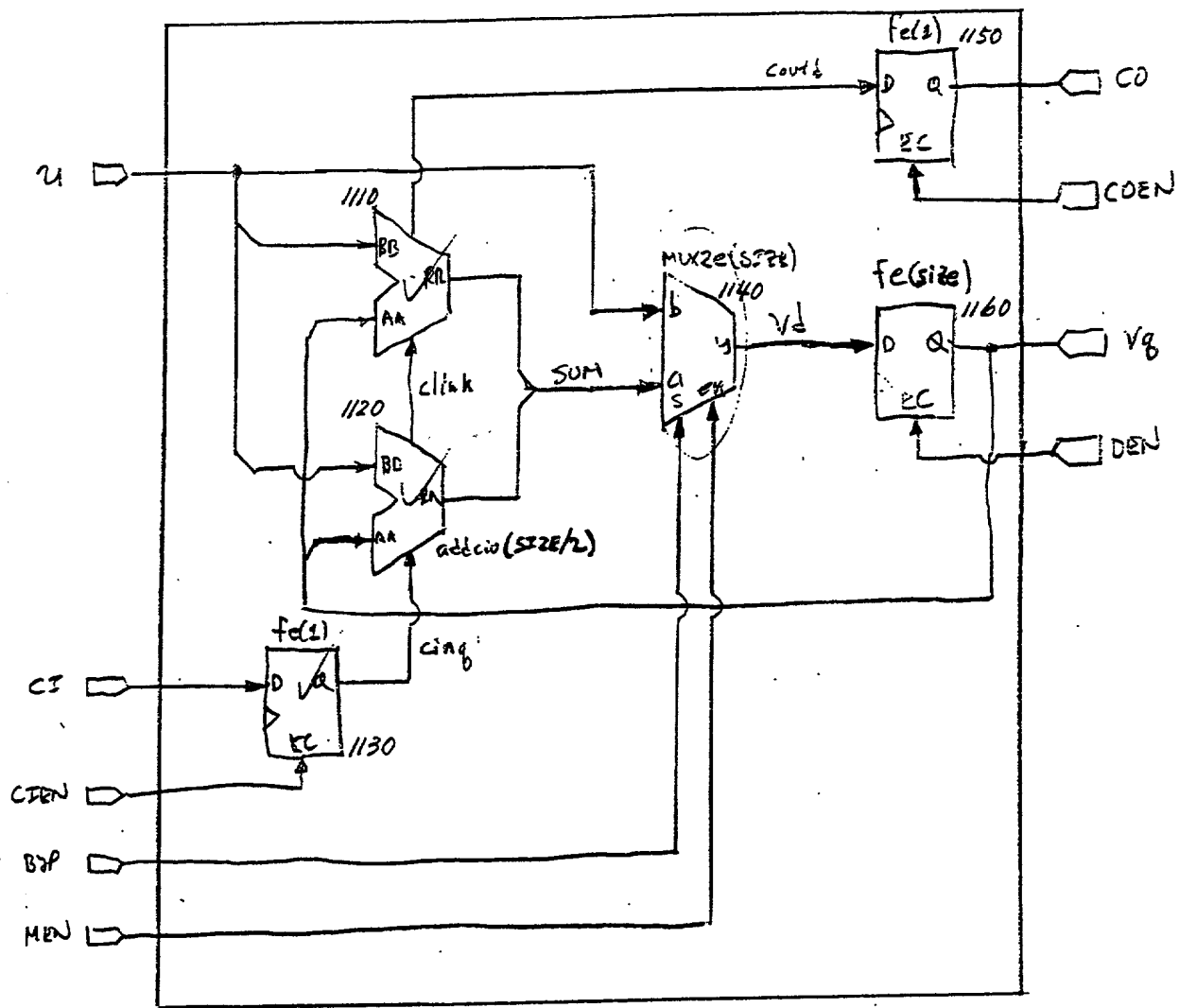


Fig. 10

522



526

Fig. 11

Banyan Switched Processor Datapath

Inventor: Michael A. Baxter

Docket No.: 20412-03873

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